a first oxide layer positioned on a substrate;

a dielectric layer having a high dielectric constant positioned on the first oxide layer;

a second oxide layer positioned on the dielectric layer having the high dielectric constant, wherein the first oxide layer, the dielectric layer having the high dielectric constant and the second oxide layer together form a charge trapping layer, wherein a band gap of the dielectric layer having the high dielectric constant is smaller than that of silicon oxide (SiO_2); and

a gate located on the second oxide layer of the charge trapping layer; and

a source/drain region located at two lateral sides of the substrate.

7. (Once Amended) A structure of a flash memory comprising:

a first oxide layer positioned on a substrate;

a dielectric layer having a high dielectric constant positioned on the first oxide layer, wherein the dielectric layer and the first oxide layer together form a charge trapping layer and the dielectric layer having the high dielectric constant is a mixture of materials selected from a group consisting of Al_2O_3, Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, Ta_2O_5, Pr_2O_3 and TiO_2;

a gate positioned on the dielectric layer having the high dielectric constant; and

a source/drain region positioned at two lateral sides of the substrate.